Biography

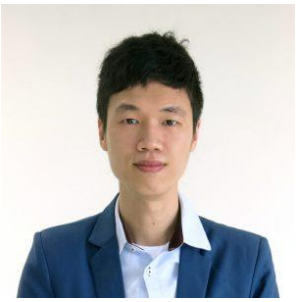
Chi-Hang Chan (S'12 M'22) received a B.S. degree in electrical engineering from University of Washington (U.W. Seattle), USA, in 2008, and an M.S. degree and Ph.D. from the University of Macau, Macao, China, in 2012 and 2015, respectively. He worked at University of California, Los Angeles (UCLA), USA as a special scientist in 2016 and served as a research assistant professor at University of Macau, Macao, China. From 2017 to 2022. He had been served as an Assistant Professor and now as Associate Professor in SKL-AMSV at University of Macau.

He received the Chipidea Microelectronics Prize and Macau Science and Technology Development Fund (FDCT) Postgraduates Award during his Master's and Ph.D. study. He also received Macau FDCT Award for Technological Invention in 2014, 2016, 2018, 2020, and 2022 for his outstanding academic and research achievements in microelectronics. He is the recipient of the 2015 Solid-State-Circuit-Society (SSCS) Pre-doctoral Achievement Award and co-recipient of the IEEE ESSCIRC 2014 Best Paper Award. His students received a number of SSCS awards, including IEEE 2021 Asian solid-state conference (A-SSCC) student design contest - distinguished design award and ISSCC 2019/2020 travel grant awards.

He holds more than 10 US/China Patents. He also has authored and co-authored 22 IEEE Journal Solid-State Circuit (JSSC), 18 IEEE International Solid-State Circuit Conference (ISSCC), 7 IEEE VLSI symposia (Circuit), and 28 IEEE Transaction (13x TCASI, 6x TCAS II, 9x TVLSI) papers in the data converter and clock circuit design field.

He serves as a reviewer in IEEE Journal Solid State Circuit (JSSC), IEEE Journal Solid State Circuit Letter (L-SSC), IEEE Transactions on Circuits and Systems I – Regular Papers (TCAS I), IEEE Transactions on Microwave Theory and Techniques (TMTT), IEEE Transactions on Circuits and Systems II – Express Briefs (TCAS II) and IEEE Transactions on Very Large Scale Integration (TVLSI). Since 2018, he has been the Secretary of IEEE Solid State Society Macau Chapter and IEEE Asian Solid-State Circuit Conference 2019. He serves as TPC in Data Converter subcommittee at IEEE A-SSCC 2023.

CURRICULUM VITAE



Chi-Hang Chan, Ivor (Ph.D., IEEE Member)

PERSONAL INFORMATION

- **Date of Birth**: 29th March 1985
- **Contact Phone Number**: (+853) 63864592
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RESEARCH INTERESTS

- High-speed Nyquist Analog-to-digital converter
  - SAR, Multi-bit SAR, Flash, Pipeline SAR and Time-domain
- Wideband Noise-shaping sigma delta modulator
  - Noise-shaping SAR and Noise-shaping pipeline SAR, Continuous time SDM
- Mixed-Signal Circuits, such as comparator, latch, DAC, etc.
- Foreground & Background Digital Calibrations
- Low-jitter Ring-Vco-Based PLLs
- ToF LiDAR System

PROFESSIONAL REVIEW SERVICES

- Journal

➢ IEEE Journal of Solid-State-Circuits
➢ IEEE Journal of Solid-State-Circuits Letter
➢ IEEE Transactions on Circuits and Systems I – Regular Papers
➢ Transactions on Power Electronics
➢ IEEE Transactions on Microwave Theory and Techniques
➢ IEEE Transactions on Circuits and Systems II – Express Briefs
➢ IEEE Transactions on Very Large Scale Integration

ACADEMIC QUALIFICATIONS

Aug 2015	**Ph.D.** in Electrical and Electronics Engineering, University of Macau Ph.D. Thesis: ***Design Techniques and Considerations in Moderate to Low Resolution Power efficient GHz Range ADCs***
Aug 2011	**M.Sc.** with Excellent Award in Electrical and Electronics Engineering, University of Macau. Average M.Sc. Thesis: ***A Study on Comparator and Offset Calibration Techniques in High-Speed Nyquist ADCs***
June 2008	**B.Sc.** in School of Electrical engineering of University of Washington, Seattle, USA.

❑ PROFESSIONAL EXPERIENCE

2022-Present	**Associate Professor** Microelectronics Key Research Area/Data Conversion Research Line, State Key Laboratory of Analog and Mixed-Signal VLSI laboratory, University of Macau.
2017-2022	**Assistant Professor** Microelectronics Key Research Area/Data Conversion Research Line, State Key Laboratory of Analog and Mixed-Signal VLSI laboratory, University of Macau.
2016	**Special Scientist** University of California, Los Angeles (UCLA), USA
2015	**Postdoctoral Fellow** Microelectronics Key Research Area/Data Conversion Research Line, State Key Laboratory of Analog and Mixed-Signal VLSI laboratory, University of Macau.
2012-2015	**Research Fellow** (funded by RC Project) Microelectronics Key Research Area/Data Conversion Research Line, State Key Laboratory of Analog and Mixed-Signal VLSI laboratory, University of Macau.
2011 –2012	**Senior Research Assistant** (funded by RC Project), Microelectronics Key Research Area/ Data Conversion Research Line, State Key Laboratory of Analog and Mixed-Signal VLSI Laboratory, University of Macau.
2009 –2011	**Master Post-graduate Studentship**, University of Macau (Assisting in Teaching and Research)
Mar 2008 – Aug 2009	**Research Assistant**, University of Macau (Assisting in Research)
Jun – Sep 2007	**Internship of** Chipidea Microelectronics, Macau (Now Synopsys Macau)

❑ PUBLICATIONS

Patents (Accepted)

1. Chi-Hang Chan, Yan Zhu, U-Fat Chio, Sai-Weng Sin, Seng-Pan U and R.P. Martins, "Comparator and Calibration Thereof," ***US Patent 8829942***
2. Yan Zhu, Chi-Hang Chan, U-Fat Chio, Sai-Weng Sin, Seng-Pan U, R.P. Martins and Franco Maloberti, "Analog to Digital Converter Circuit," ***US Patent 8659461***
3. Yan Zhu, Chi-Hang Chan, Sai-Weng Sin, Seng-Pan U, R.P. Martins and Franco Maloberti, "N-bits Successive Approximation Register Analog-to-digital Converting Circuit ," ***US Patent 8344931 B2***
4. Yan Zhu, Chi-Hang Chan, Sai-Weng Sin, Seng-Pan U and R.P. Martins, "Sampling Front-end for Analog to Digital Converter," ***US Patent 8947283***.
5. Sai-Weng Sin, Li Ding, Yan Zhu, He-Gong Wei, Chi-Hang Chan, U-Fat Chio, Seng-Pan U, R.P.Martins and F.Maloberti, "Time-interleaved Pipeline-SAR Analog to Digital Converter with Low Power Consumption" ***US Patent 8427355 B2***
6. Xing Kai, Yan Zhu, Chi-Hang Chan, R.P.Martins, "单运放二阶滤波器电路" ***China Patent ZL 202122800711.8***

7. Sai-Weng Sin, Li Ding, Yan Zhu, He-Gong Wei, Chi-Hang Chan, U-Fat Chio, Seng-Pan U, R.P.Martins and F.Maloberti, "Analog-to-digital Converter Circuit" ***TW Patent 1446723 B***

Journal Solid-State Circuits (JSSC) Papers:

1. Chi-Hang Chan, Yan Zhu, W. Zhang, S. U and R. P. Martins, "A Two-Way Interleaved 7-b 2.4-GS/s 1-Then-2 b/Cycle SAR ADC With Background Offset Calibration," in IEEE *Journal of Solid-State Circuits*, vol. 53, no. 3, pp. 850-860, March 2018.
2. Chi-Hang Chan, Yan Zhu, W. Zhang, S. U and R. P. Martins, "60-dB SNDR 100-MS/s SAR ADCs With Threshold Reconfigurable Reference Error Calibration," in IEEE *Journal of Solid-State Circuits*, vol. 52, no. 10, pp. 2576-2588, Oct. 2017.
3. Chi-Hang Chan, Yan Zhu, Sai-Weng Sin, Seng-Pan U and R.P. Martins, "A 5.5mW 6-b 5GS/s 4-Interleaved 3b/cycle SAR ADC in 65nm CMOS," in IEEE *Journal of Solid-State Circuits*, Vol. 51, no. 2, pp. 365-377, Feb. 2016
4. Chi-Hang Chan, Yan Zhu, Sai-Weng Sin, Seng-Pan U, R.P. Martins and Franco Maloberti, "A 5b 1.25GS/s 4X Capacitive Folding Flash ADC in 65nm CMOS," in IEEE *Journal of Solid-State Circuits* , Vol. 48, no. 9, pp. 2154 -2169, Sep. 2013.
5. Y. Zhang, J. Zhang, S. Liu, R. Ding, Yan Zhu, Chi-Hang Chan and R. P. Martins ., "A 20 MHz Bandwidth 79 dB SNDR SAR-Assisted Noise-Shaping Pipeline ADC With Gain and Offset Calibrations," in *IEEE Journal of Solid-State Circuits*, vol. 57, no. 3, pp. 745-756, March 2022.
6. H. Zhang, Yan Zhu, Chi-Hang Chan and R. P. Martins, "An Inherent Gain Error Tolerance Noise-Shaping SAR-Assisted Pipeline ADC With Code-Counter-Based Offset Calibration," in *IEEE Journal of Solid-State Circuits*, vol. 57, no. 5, pp. 1480-1491, May 2022.
7. Z. Zheng, L. Wei, J. Lagos, E. Martens, Yan Zhu, Chi-Hang Chan, J. Craninckx, and R. P. Martins, "A 3.3-GS/s 6-b Fully Dynamic Pipelined ADC With Linearized Dynamic Amplifier," in *IEEE Journal of Solid-State Circuits*, vol. 57, no. 6, pp. 1673-1683, June 2022.
8. Y. Song, Y. Zhu, Chi-Hang Chan and R. P. Martins, "A 40-MHz Bandwidth 75-dB SNDR Partial-Interleaving SAR-Assisted Noise-Shaping Pipeline ADC," in *IEEE Journal of Solid-State Circuits*, vol. 56, no. 6, pp. 1772-1783, June 2021.
9. M. Zhang, Yan Zhu, Chi-Hang Chan and R. P. Martins, "An 8-Bit 10-GS/s 16× Interpolation-Based Time-Domain ADC With <1.5-ps Uncalibrated Quantization Steps," in *IEEE Journal of Solid-State Circuits*, vol. 55, no. 12, pp. 3225-3235, Dec. 2020.
10. W. Jiang, Y. Zhu, M. Zhang, Chi-Hang Chan and R. P. Martins, "A Temperature-Stabilized Single-Channel 1-GS/s 60-dB SNDR SAR-Assisted Pipelined ADC With Dynamic Gm-R-Based Amplifier," in *IEEE Journal of Solid-State Circuits*, vol. 55, no. 2, pp. 322-332, Feb. 2020.
11. W. Wang, Chi-Hang Chan, Y. Zhu and R. P. Martins, "A 100MHz BW 72.6dB-SNDR CT ΔΣ Modulator Utilizing Preliminary Sampling and Quantization," in *IEEE Journal of Solid-State Circuits*, vol. 55, no. 6, pp. 1588-1598, June 2020.
12. Y. Song, Chi-Hang Chan, Y. Zhu and R. P. Martins, "A 12.5-MHz Bandwidth 77-dB SNDR SAR-Assisted Noise Shaping Pipeline ADC," in *IEEE Journal of Solid-State Circuits*, vol. 55, no. 2, pp. 312-321, Feb. 2020.
13. M. Zhang, Chi-Hang Chan, Y. Zhu and R. P. Martins, "A 0.6-V 13-bit 20-MS/s Two-Step TDC-Assisted SAR ADC With PVT Tracking and Speed-Enhanced Techniques," in *IEEE Journal of Solid-State Circuits*, vol. 54, no. 12, pp. 3396-3409, Dec. 2019.
14. W. Wang, Yan Zhu, Chi-Hang Chan and R. P. Martins, "A 5.35-mW 10-MHz Single-Opamp Third-Order CT$\Delta\Sigma$Modulator With CTC Amplifier and Adaptive Latch DAC Driver in 65-nm CMOS," in IEEE Journal of Solid-State Circuits, vol. 53, no. 10, pp. 2783-2794, Oct. 2018.
15. Yan Zhu, Chi-Hang Chan, S. P. U and R. P. Martins, "An 11b 450 MS/s Three-Way Time-Interleaved Subranging Pipelined-SAR ADC in 65 nm CMOS," in *IEEE Journal of Solid-State Circuits*, vol. 51, no. 5, pp. 1223-1234, May 2016.
16. Yan Zhu, Chi-Hang Chan, Sai-Weng Sin, Seng-Pan U, Rui Paulo Martins, Franco Maloberti, "A 35fJ 10b 160 MS/s Pipelined-SAR ADC with Self-Embedded Offset Cancellation" in IEEE *Journal of Solid-State Circuits*. Vol. 47, no. 11, pp. 2614 -2626, Nov. 2012.
17. Hegong Wei, Chi-Hang Chan, U-Fat Chio, Sai-Weng Sin, Seng-Pan U, R.P. Martins and Maloberti, F., "An 8-b 400-MS/s 2-b-Per-Cycle SAR ADC With Resistive DAC," in IEEE *Journal of Solid-State Circuits*, vol.47, no.11, pp.2763,2772, Nov. 2012.

18. Yan Zhu, Chi-Hang Chan, U-Fat Chio, Sai-Weng Sin, Seng-Pan U, R.P. Martins and Franco Maloberti, "A 10-bit 100-MS/s Reference-Free SAR ADC in 90nm CMOS," in IEEE *Journal of Solid-State Circuits*, vol. 45, no. 6, pp. 1111 -1121, Jun 2010.

International Solid-State Circuits Conference (ISSCC) Papers:

1. Chi-Hang Chan, Yan Zhu, I.M. Ho , W.H. Zhang, S. P. U; R. P. Martins "A 5mW 7b 2.4GS/s 1-then-2b/cycle SAR ADC with Background Offset Calibration," *IEEE International Solid-State Circuits Conference (ISSCC),* pp. 282-283, Feb 2017.
2. Chi-Hang Chan; Yan Zhu; Sai-Weng Sin; Seng-Pan, U.; Martins, R.P., "A 5.5mW 6b 5GS/S 4×-interleaved 3b/cycle SAR ADC in 65nm CMOS," in IEEE *International Solid-State Circuits Conference - (ISSCC)*, pp.1-3, Feb. 2015.
3. Y. Cao; M. Zhang; Yan Zhu; Chi-Hang Chan; R. P. Martins, "A Single-Channel 12b 2GS/s PVT-Robust Pipelined ADC with Critical-damp Ring Amplifier and Time-Domain Quantizer," Accepted in *IEEE International Solid- State Circuits Conference (ISSCC)*, Feb. 2023.
4. H. Zhao, M. Zhang, Yan Zhu; Chi-Hang Chan; R. P. Martins, "A 2x times-Interleaved 9b 2.8GS/s 5b/cycle SAR ADC with Linearized Configurable V2T Buffer Achieving 50dB SNDR at 3GHz Input," Accepted in *IEEE International Solid- State Circuits Conference (ISSCC)*, Feb. 2023.
5. H. Zhang, Yan Zhu, Chi-Hang Chan, R. P. Martins, "A 25MHz-BW 77.2dB-SNDR 2nd-Order Gain-Error-Shaping and NS Pipelined SAR ADC Based on a Quantization-Prediction-Unrolled Scheme," Accepted in *IEEE International Solid- State Circuits Conference (ISSCC)*, Feb. 2023.
6. J. Hao, M. Zhang, Y. Zhang, S. Liu, Z. Zhu, Yan Zhu, Chi-Hang Chan, R. P. Martins, "A Single-Channel 2.6GS/s 10b Dynamic Pipelined ADC with Time-Assisted Residue Generation Scheme Achieving Intrinsic PVT Robustness," Accepted in *IEEE International Solid- State Circuits Conference (ISSCC)*, Feb. 2023.
7. Y. Zhang, J. Hao, S. Liu, Z. Zhu, Yan Zhu, Chi-hang Chan*, R. P. Martins, "A Single-Channel 70dB-SNDR 100MHz-BW 4th-Order Noise-Shaping Pipeline SAR ADC with Residue Amplifier Error Shaping," Accepted in *IEEE International Solid-State Circuits Conference (ISSCC)*, Feb. 2023.
8. H. Zhang; Yan Zhu; Chi-Hang Chan; R. P. Martins, "27.6 A 25MHz-BW 75dB-SNDR Inherent Gain Error Tolerance Noise-Shaping SAR-Assisted Pipeline ADC with Background Offset Calibration," in *IEEE International Solid- State Circuits Conference (ISSCC)*, pp. 380-382, Feb. 2021.
9. Y. Song; Yan Zhu; Chi-Hang Chan; Martins, R.P., "A 2.56mW 40MHz-Bandwidth 75dB-SNDR Partial-Interleaving SAR-Assisted NS Pipeline ADC With Background Inter-Stage Offset Calibration," in IEEE *International Solid-State Circuits Conference - (ISSCC)*, Feb. 2020.
10. M. Zhang; Yan Zhu; Chi-Hang Chan; Martins, R.P., "A 4× Interleaved 10GS/s 8b Time-Domain ADC with 16× Interpolation-Based Inter-Stage Gain Achieving >37.5dB SNDR at 18GHz Input," in IEEE *International Solid-State Circuits Conference - (ISSCC)*, Feb. 2020.
11. Zihao Zheng; Lai Wei; Jorge Lagos; Ewout Martens; Yan Zhu; Chi-Hang Chan; Jan Craninckx; Rui P. Martins, "A Single-Channel 5.5mW 3.3GS/s 6b Fully Dynamic Pipelined ADC with Post-Amplification Residue Generation," in IEEE *International Solid-State Circuits Conference - (ISSCC)*, Feb. 2020.
12. M. Zhang; Chi-Hang Chan; Yan Zhu; Martins, R.P., "A 0.6V 13b 20MS/s Two-Step TDC-Assisted SAR ADC with PVT Tracking and Speed-Enhanced Techniques," in IEEE *International Solid-State Circuits Conference - (ISSCC)*, Feb. 2019.
13. W. Wang; Chi-Hang Chan; Yan Zhu; Martins, R.P., "A 72.6dB-SNDR 100MHz-BW 16.36mW CTDSM with Preliminary Sampling and Quantization Scheme in Backend Subranging QTZ, " in IEEE *International Solid-State Circuits Conference - (ISSCC)*, Feb. 2019.
14. X. Yang; Chi-Hang Chan; Yan Zhu; Martins, R.P., "A -246dB Jitter-FoM 2.4GHz Calibration-Free Ring-Oscillator PLL Achieving 9% Jitter Variation Over PVT, " in IEEE *International Solid-State Circuits Conference - (ISSCC)*, Feb. 2019.
15. W. Jiang; Yan Zhu; M. Lei; Chi-Hang Chan; Martins, R.P., "A 7.6mW 1GS/s 60dB SNDR Single-Channel SAR-Assisted Pipelined ADC with Temperature-Compensated Dynamic Gm-R-Based Amplifier," in IEEE *International Solid-State Circuits Conference - (ISSCC)*, Feb. 2019.
16. He-Gong Wei, Chi-Hang Chan, U-Fat Chio, Sai-Weng Sin, Seng-Pan U, R. P. Martins and F. Maloberti, "A 0.024mm2 8-bit 400 MS/s SAR ADC with 2-bit per Cycle and Resistive DAC in 65 nm CMOS," in IEEE *International Solid-State Circuit Conference (ISSCC)*, pp.187-189, Feb 2011.

❑ PROFESSIONAL AFFILIATIONS

2012 – 2015	IEEE Student Member
2015 – Present	IEEE Member
2018 – Present	IEEE Solid State Society Macau Chapter Secretary
2019	IEEE Asian Solid-State Circuit Conference 2019 Secretary

❑ HONORS AND AWARDS

2022	Macau Science and Technology Development Fund Award for Technological Invention (1st Inventor)
2021	Distinguished Design Award from Student Design Contest of IEEE Asian Solid-state Circuits conference (Supervised student)
2020	Macau Science and Technology Development Fund Award for Technological Invention (1st Inventor)
2018	Macau Science and Technology Development Fund Award for Technological Invention
2016	Macau Science and Technology Development Fund Award for Technological Invention
2015	IEEE Solid-State-Circuit Society Pre-doctoral Achievement Award (1st author)
2014	Best Paper Award in IEEE European Solid-state Devices and Circuits conference (2nd author)
2014	Macau Science and Technology Development Fund Award for Technological Invention
2014	Macau Science and Technology Development Fund Postgraduate student award (Ph.D.)
2012	VLSI Symposia Circuit travel award (1st author)
2011	Macau Science and Technology Development Fund Postgraduate student award (Master)
2009	Chipidea Microelectronics Prize
2005 ~ 2006	Dean's list, University of Washington